REMARKS

Amendment to the claims

Claims 2, 4 and 6 have been clarified by reciting *"wells of a second conductivity type"*. Applicants note that the specification as filed describes N-type wells and P-type wells, for example in paragraph [0046], and teaches unambiguously that the wells' "second type" originally recited in claims 2, 4 and 6, is a second conductivity type. Accordingly, Applicants note that the above amendment of claim 2, 4 and 6 is a mere clarification of the claims, not a limitation of their scope.

Claim 3 has been clarified by reciting that *"at least one of said plurality of wells is separated from said first well ~~by a minimum first conductivity type to second conductivity type separation~~"*. Applicants note that the present wording of claim 3 is supported by the application as filed, for example Fig. 5d and the corresponding portion of the specification.

Claim 6 has been amended to correspond to the figures as filed.

No new matter has been added. Applicants expressly reserve the right to prosecute any matter cancelled from the claims in this application or in any derivative thereof.

Objections to the drawings

The drawings stand objected to as failing to comply with 37 CFR 1.83(a) for failing to show the features recited in claim 6. Applicants respectfully submit that the features recited in claim 6 as amended are shown in the figures as filed. For example, Fig. 5d shows: *"A semiconductor circuit comprising: a substrate (12) having a first well (22) of a first conductivity type; a gate region (19) being arranged above the first well (22); a plurality of active regions (16a, 18a) of said first conductivity type disposed in said substrate (12), at least two (16a, 18a) of said plurality of active regions being separated from one another by, and in physical contact with, said first well (22) of said first conductivity type disposed in said substrate (12) under said gate region (19); and a plurality of wells (14a, 14b) of a second conductivity type being partially disposed under said at least two of said plurality of active regions (16a, 18a),*

wherein said plurality of wells (14a, 14b) of a second conductivity type are separated from said first well (22)".

Accordingly, Applicants respectfully request the Examiner to withdraw this objection.

Objection to the specification

The disclosure stands objected to because of a misspelling of the word "turned" on page 10, line 5 and because of the improper terms "microscopic investigates" on page 18, line 9. Applicants note that paragraph [0038] of the specification, including page 10, line 5, has been corrected with the proper spelling of the word "turned", and that paragraph [0056] of the specification, including page 18, line 9, has been corrected to recite "microscopic investigations". Accordingly, Applicants respectfully request the Examiner to withdraw this objection.

Objection to the claims

Claims 2, 4 and 6 stand objected to for reciting the terms "second type". Applicants note that pursuant to the request of the Examiner, the word "conductivity" has been recited between the words "second" and "type". Accordingly, Applicants respectfully request the Examiner to withdraw this objection.

Rejection under 35 U.S.C. 112

Claim 3 stand rejected under 35 U.S.C. 112, second paragraph, for reciting the terms *"separated from said first well by a minimum first conductivity type to second conductivity type separation"*. Applicants note that the terms *"a minimum first conductivity type to second conductivity type separation"*, deemed unclear by the Examiner, have been cancelled. Accordingly, Applicants respectfully request the Examiner to withdraw this rejection.

Rejection under 35 U.S.C. 102

Claims 1 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,912,053 to Schrantz. Applicants respectfully disagree.

Claim 1

Applicants acknowledge that Schrantz discloses a structure having a gate region 130, a first active region 140, a second active region 142, and a channel region (well) 128 which "provides an electrical path between the source and drain regions".

However, Applicants note that the structure of Schrantz is a functional JFET with improved speed and reduced size (column 2, lines 3-4), and that accordingly, as is well known in the art, when the gate-source voltage of the JFET reaches its pinchoff voltage, the channel region 128 has practically infinite resistance, and then no longer provides an electrical path between the sources and drain regions.

Applicants further note that paragraph [0035] of the specification define a *"reasonable voltage"* as *"any gate voltage found in normal device operation such that the voltage does not break down the gate oxide 21"*. Applicants note that, since a functional JFET is designed to not be destroyed upon application of its pinchoff voltage to its gate, the pinchoff voltage of a JFET is a reasonable voltage as defined in the present application.

In view of the above, Applicants submit that Schrantz cannot be deemed to disclose or suggest that the channel region 128 *"provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit"*.

Accordingly, Applicants respectfully submit that claim 1 is patentable over Schrantz.

Claim 5

Claim 5 depends on claim 1. Applicants respectfully submit that at least in view of its dependency on claim 1, claim 5 is patentable over Schrantz.

Rejection under 35 U.S.C. 103

Claims 2, 3 and 4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Schrantz in view of U.S. Pat. No. 3,938,620 to Spadea, and claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Schrantz in view of U.S. Pat. No. 6,373,106 to Maki. Applicants respectfully disagree.

Claims 2, 3 and 4

Claims 2, 3 and 4 depend directly or indirectly on claim 1. Applicants note that the Examiner has failed to show that Spadea shows a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit"*. In view of the above, Applicants submit that the Examiner has failed to show that Schrantz or Spadea, alone or in combination, would have led one of ordinary skill to a structure as recited in claim 1, and in particular *"wherein said first well provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit"*. Accordingly, Applicants respectfully submit that claim 1 is patentable over Schrantz in view of Spadea, and respectfully submit that at least in view of their dependency on claim 1, claims 2, 3 and 4 are patentable over Schrantz in view of Spadea.

Claim 6

The Examiner acknowledges that Schrantz does not disclose *"a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second conductivity type are separated from said first well"*.

The Examiner states that Maki discloses a semiconductor device comprising N-source/drain regions 4 and P-wells 3b, and asserts that it would have been obvious to one of ordinary skill in the art to dispose the plurality of wells of Maki under the active regions of Schrantz in order to isolate the transistor of Schrantz from other elements. Applicants respectfully disagree.

Applicants note that Maki is limited to a structure comprising at least two transistors of a same conduction type (e.g. column 4, lines 28-31; claims), whereas

Schrantz is not limited to such a restrictive feature. Accordingly, Applicants submit that one of ordinary skill in the art having the knowledge of Schrantz would have been discouraged to look for improvements of the structure of Schrantz in a structure as restrictive as Maki's. Applicants also submit that it would be far from obvious to one skilled in the art that any feature of Maki, such as the wells 3b of one of the at least two transistors, excerpted from the specific at-least-two-transistors-of-the-same-type environment of Maki, would still operate in Schrantz as described in Maki.

In addition, Applicants note that Fig. 5 of Maki shows an embodiment wherein P-wells 3b are formed under isolation regions 2 and not in contact with source/drain regions 4 (column 9, lines 59-62), so that "the element separation characteristic may be further improved" and "the semiconductor elements can further be reduced in size" (column 10, lines 30-37). Accordingly, Applicants submit that, even if notwithstanding the hurdles above, one of ordinary skill in the art had decided to excerpt some features from Maki and try applying them to Schrantz, and if one skilled in the art had looked for a way to improve the isolation of the transistor of Schrantz from other elements, one would logically have turned to the embodiment of Maki offering the best isolation (and size reduction, since size reduction is an important object of Schrantz), and would have used the P-wells 3b of Fig. 5 of Maki. The P-wells 3b of Fig. 5 of Maki do not contact the active regions, and a combination of such wells and of the structure of Schrantz would therefore not have anticipated a structure as recited in claim 6, and in particular having *"a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions"*.

At least in view of the above, Applicants submit that claim 6 is patentable over Schrantz in view of Maki.

* * *

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees that may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as

including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

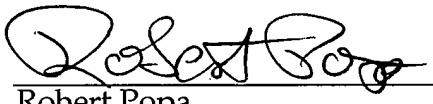
August 31, 2005
(Date of Transmission)

Shannon Tinsley
(Name of Person Transmitting)


(Signature)

8/31/05
(Date)

Respectfully submitted,



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